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ANALYSIS ON EXECUTING ALU OPERATIONS, PARITY-PRESERVING GATES ARE SORT BY VERILOG HDL AND STIMULATED USING XILINX SOFTWARE

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ABSTRACT
With the development of MOSFETs in the 1960s, the semiconductor industry has seen great improvements due to device scalability, in respect to speed and functionality, but power dissipation has also been a significant issue. Researchers are perception for a game-changing approach since gadget scaling has hit its limit. Reversible computing is one of the VLSI industry's growing topics. This technology's zero power scattering in revocable logic circuits has drawn the attention of researchers in major part. Here, research into creating an ALU with reversible quantum gates is being suggested. The proposed ALU can execute simultaneous arithmetic and logical operations, either might be selected based on the circumstances, and is capable of identifying a single bit error. The parity-preserving gates Fredkin and CNOT are employed in the architecture. Verilog HDL is used to generate the suggested design, and Xilinx software is used to excite it. Minimizing the number of gates, quantum cost, garbage outputs, and auxiliary inputs or input constants is the design's primary goal.

INTRODUCTION

Reversible circuit synthesis has recently become more and more important, offering alternatives to traditional Boolean networks. Two significant findings served as the impetus for reversible computing. Such circuits have two advantages over conventional circuits: first, they consume less energy, and second, they are intimately related to a number of cutting-edge technologies like quantum circuits. In 1961, Landauer demonstrated that irreversible circuits always use power and release heat at a minimum rate of kTln2 for any little amount When k is the Boltzmann value and T stands for temperature, information's erasure. Later, Bennett demonstrated that theoretically, dissipation of energy of any size, or even zero, is only feasible if absolutely no data is lost while computing. As input and output data are handled while losing any of the original data, this is advantageous for reversible circuits. Although information loss accounts for a minor portion of facility expenditure in present VLSI circuits, this is frequently anticipated to change as packing 2 densities rise, reducing facility expenditure per gate operation and creating a lovely alternative in bidirectional computation. Given that reversal is an integral component of quantum computing, researching reversible circuits enhances our understanding of this field. Reversal circuits are also used in adiabatic circuits, cryptography, optical computing, digital signal processing, low power CMOS designs, and other fields.

EXISTING METHOD AND PROPOSED METHOD

In computation, an arithmetic and logic unit may be a combination al digital circuit that executing arithmetic and logical operations. An ALU consists of Adder, Subtractor, Multiplexer, Demultiplexers, Shift registers etc. And are designed with MOSFET transistors. The MOSFET transistors utilized in digital circuits, which uses irreversible logic gates. And it's certain limitations like more power dissipation, space consumption, and propagation delay.

PROPOSED METHOD

In proposed method, a Parity-preserving gates are used in the construction of 4-bit ALU technology. Since there can be no bit loss in irreversible computing, there is probably zero or very little power consumption. In this case, parity checking in bidirectional gates may be employed to find flaws. Here, the Modelsim, which logic simulator or ISIM is utilized for system-level testing whereas Xilinx ISE is predominantly employed for circuit synthesis and design. Comparing to the current ALU designs, the design exhibits improvement in all metrics evaluated for assessment.

Reversible circuits:

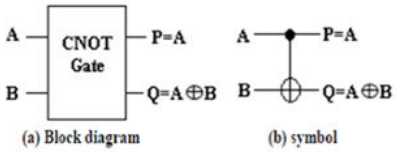
A great deal of study is done on irreversible circuits in an effort to find an alternative to traditional design. To make it easier to create and test circuits, and in particularly to use them in various computing fields, some special qualities of reversible logic are recognized. Reversible logic is connected to quantum circuits through the use of reversible gates' quantum realizations.

Reversible function:

Every input vector translates bijectively to a single output vector in a nxn bidirectional circuit, which implements an n-input/n-output function. The bidirectional circuits don't permit feedback or fan-out.

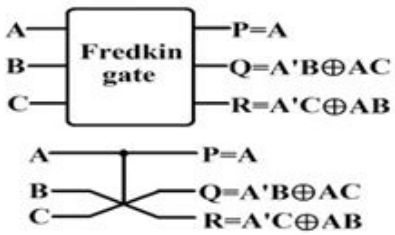
There are two ways that irreversible functions vary compared to their reversible equivalent. First, there are not an equal number of inputs and outputs. A bidirectional gate is an N-input, N-output logic component that maps each input to each output in at least one way. It aids us in both determining the outputs from the inputs and in individually recovering the inputs through the outputs. Parity-preserving gates are another name for irreversible logic gates. maintaining parity Bidirectional logic gates are within the category of bidirectional logic gates and have the additional characteristic that the parity of the input and output are the same. If the EXOR of the inputs and the EX-OR of the outputs match, a bidirectional gate will preserve parity.

The gates used in this project are CNOTGATE-The controlled NOT gate is aquantum logic gate. The another name of CNOT gate is Feynmann gate.Thisis2x2matrixofinputsandoutputs.Oneoutputissameas the input and the another output is xor operation of inputs. The CNOT gate is demonstrated in below fig(1).



Fig(1):CNOT Gate

A FREDKIN gate has three inputs and three outputs. The result is a synthesis of different logic's including and, or, and xor. Other digital logic's that the CNOT gate is unable to implement are implemented using this gate. It has a high quantum expense of five. Fig. 2 displays the logic operation that the Fredkin gate executed.



Fig(2): Fred kin Gate

Reversible arithmetic and logic unit:

The arithmetic logic unit is a multipurpose circuitry that, in response to control inputs, can carry out any of a number of potential operations on both operands A and B.

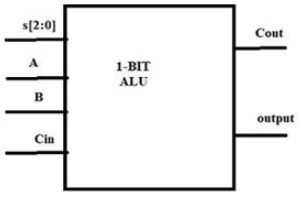
The module's design allows customization at less gate costs than building multiple single-function circuits. But combining many tasks into a single unit necessitates more control lines and circuit resources.

In the present paper, a bidirectional ALU with traditional irreversible ALU functions is implemented. For the ALU design, we should focus on which includes as many arithmetic and logical operations is feasible into a straightforward structure that is as efficient and inexpensive as possible.

As a result, the majority of procedures accessible in traditional irreversible ALU are included in the reversible ALU provided above.

1-BIT ARITHMETIC AND LOGIC UNIT

The formal diagram of single- bit RALU is demonstrated in below illustration.

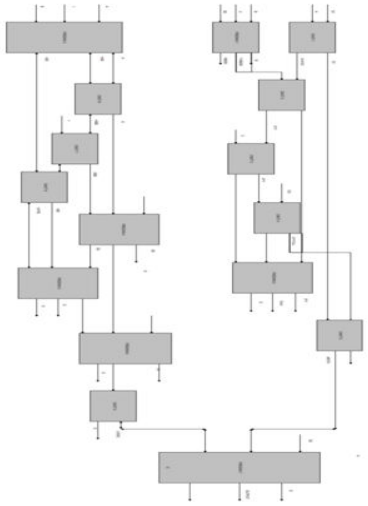


Fig(4.1):1-bitALU

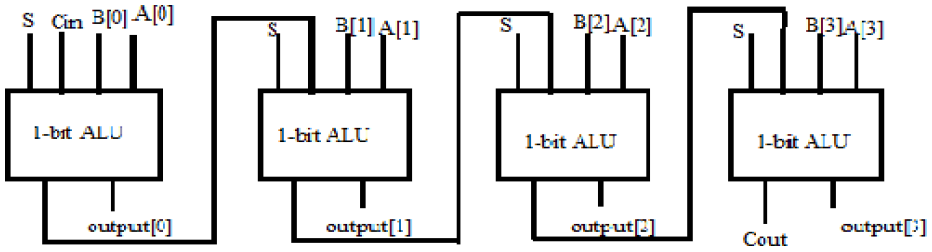
ThebelowFig.(4.2)showsthearchitectureofsingle-bitReversibleArithmeticandLogicalunitexploitationCNOTandFredkingates.AndTable4.3showstherealitytableof Fig.4.2. Through the use of parity-preserving Fredkin and CNOT gates, an innovative one-bit ALU architecture is intended. The actual table for the ALU design is shown in Table 1. The control signal S2 is responsible for choosing between the arithmetic and logical outputs. The Fredkin gate utilised has three inputs and a sum, as previously explained. A CNOT gate contains two inputs, several outputs, and additional outputs. The suggested ALU's architecture is shown in Fig. 3.2, whereby the top portion is the arithmetic unit and, consequently, the bottom portion is the logical unit. The auxiliary inputs are represented by the 1s and 0s at the input sides of the gates in Figure 6, while the garbage outputs are represented by G. For comprehending the intermediate operations of a 1 bit ALU, intermediate results are additionally shown.Fredkin and CNOT gates are employed in the design. Based on the selection signal, Fredkin gate 7 chooses an arithmetic or logical unit. S0, S1, S2, and Cin are the bits needed to choose the sort of necessary operation, and A and B are the inputs. The architecture has a 44-percent quantum cost, 16-percent gates, 4-percent constant or auxiliary inputs, and 11-percent trash output. Comparing to the prior ALU designs, the current one has made significant strides on all metrics used for evaluation.

S2	S1	S0	Cin	Operation
0	0	0	0	A
0	0	0	1	A+1
0	0	1	0	A+B
0	0	1	1	A+B+1
0	1	0	0	A
0	1	0	1	A-1
0	1	1	0	A-B
0	1	1	1	A-B-1
1	0	0	0	A|B
1	0	0	1	~(A|B)
1	0	1	0	A&B
1	0	1	1	~(A&B)
1	1	0	0	~(A^B)
1	1	0	1	A^B
1	1	1	0	A
1	1	1	1	~A

Table(4.3):Truthtableof1-bitRALU



Fig(4.2):1-BitRALUArchitecture



Fig(4.4):Schematicof4-bit RALU

ADVANTAGES

- Duplication of input through output.
- Recovers bit-loss.
- Heat management.
- Energy dissipationis less.
- Power management.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.

Designing low power arithmetic and data path for Multiple operations in a single cycle.

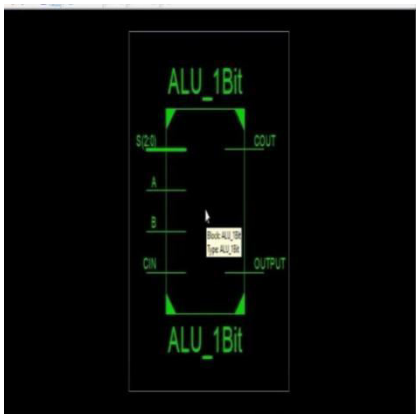
DISADVANTAGES

- Yet, the bidirectional machine has to actually run reversed to achieve its initial state in order to reap the advantages of reversible computation. If this phase is skipped, the system often fills up with digital heat and cannot continue to do additional productive tasks.
- If there are any flaws in our processing, the machine running reversed could cause chaos, so we must ensure that this didn't happen.

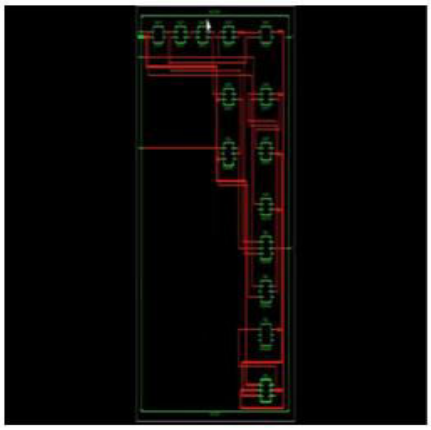
- The synthesis of reversible circuits is restricted to‘Fan-out’and‘Feedback’.

Results:

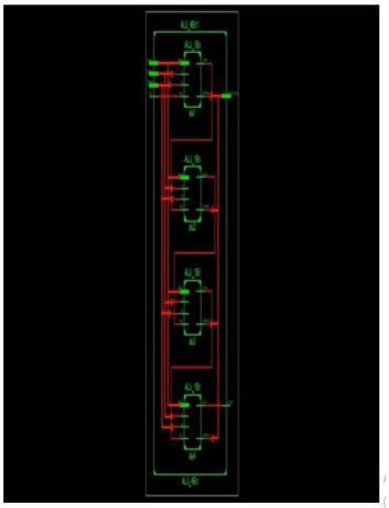
Using a simulation, we verified the reversible functioning for the suggested reversible ALU implementation (Fig. 6.3 design of reversible 4 bit ALU). Utilising Verilog HDL and Xilinx software, the design's functional verification is carried out. This suggests that, in comparison to the previous design, the new design performs better overall. Reversible logic must have a comparable number of inputs and outputs as inputs, and this requirement is met. The enhancement is in garbage outputs and constant inputs. The waste outputs were likewise reduced by 31.25%, while the auxiliary inputs dropped by 66.67%.



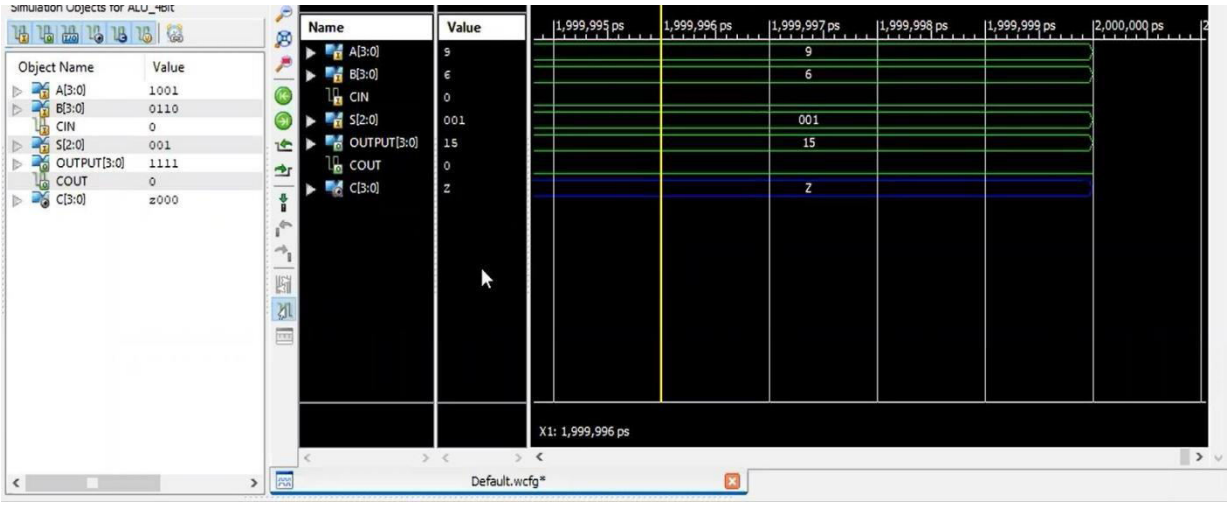
Fig(6.1):Schematic of reversible 1-bit ALU



Fig(6.2):Design of reversible 1-bit ALU



Fig(6.3):Design of reversible 4-bit ALU



Fig(6.4) Representation of 4-bit ALU

A 4-bit RALU's randomized simulator is shown in Fig.6.4 following. The output node displays whether the command signals have been followed. We compare the outputs and inputs for each control combination to random values. For instance, the output produces 1111 for control S2S1S0=001 with inputs A=1001 and B=0100 because the RALU executes an ADD operations. Keep in mind that the waste production is concealed in the presentation.

Conclusion

Irreversible logic gates and their three parameters—ancillary inputs, trash outputs, and quantum cost—have been discussed in detail in this study. The parity-preserving Fredkin and CNOT gates are addressed together using current bidirectional gates. In order to test the ALU's performance in Xilinx, Verilog HDL was used during design and implementation. Analysis of the results led to increased effectiveness. It is possible to develop multiple bit ALUs with concurrent processing using this architecture.

Future Scope

Functionality could be developed higher in the creation of cutting-edge digital design work. Building quantum

processors is an alternative because Moore's law restricts the capabilities of future computer chips. Developing a novel bidirectional gate and incorporating bidirectional logic into a full Quantum processor that is able to perform ultra-high velocity and infinitely low power computation is our subsequent study focus.

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