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EMPLOYING A FINFET-BASED SELF-CONTROLLED VOLTAGE LEVEL APPROACH, AN ANALYTICAL INVESTIGATION OF A SRAM CELL WITH LOW LEAKAGE POWER

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ABSTRACT
Devices with low power consumption are crucial in the present technological era of miniaturized circuits. In the newest technological devices, memory is crucial. As technology advanced, it became more challenging to maintain memory in terms of power usage, stability, and speed. The sub-threshold discharge current contributes importantly to the general power dissipation because of scaling. In this research, a Fin FET-based self-controllable voltage level (SVL) approach for low leakage power Static Random-Access Memory (SRAM) cells is projected. This work describes the use of the Self-Controllable Voltage Level (SVL) Method to cut down leakage power dissipation in an SRAM cell using Fin FETs. Reduced overall power dissipation is possible by applying SVL switch that can work either by reducing supply voltage to cell in standby state i.e. upper SVL or by increasing voltage of ground node connected to cell in standby state i.e. lower SVL or by a combination of both. The Fin FET based SRAM cell by this SVL switch circuit can shows aim proved execution and low leakage power compared to both conventional SRAM cell and Fin FET supported SRAM cell.
Key Words: Leakage power, SRAM, Fin FET, Self-Controllable Voltage Level (SVL), low power consumption.

1. INTRODUCTION

Long ago, the competitive market environment pushed the threshold voltage scaling and CMOS technological characteristics to achieve higher performing small devices. VLSI designers are worried with leakage power dissipation as a result of the continual scaling of CMOS devices [1]. Sub-threshold leakage current increases when the device is turned off as the feature size, or channel length, decreases. Due to the transistor not being entirely switched off, the scaling of the threshold voltage also has a significant impact on raising the sub threshold leakage current [2]. As compared to a threshold voltage that was high enough, this sub-threshold current was tiny and only made up a diminutive percentage of the power dispersion. Scaled devices have sub-threshold current that is comparable to other circuit currents and thus, the consequent sub-threshold Leakage of information is a big deal. Furthermore, efforts to reduce the size of the devices will undoubtedly result in a greater fraction of the device's overall electrical usage [3]. Any the system's power dissipation includes significant input from the SRAM cell. SRAM cells are used in memory caches, tagArrays, buffers, and numerous other CPU components [4]. Leakage represents an important concern in deep submicron CMOS manufacturing because of the scaling of channel length, gate oxide thickness, and threshold voltage. Theoretically, an upsurge in static power is possible as technologies is scaled up further [5]. Leakage electricity will contribute 50% of the total power in the future. Static power is lost for all FET-based transistors as a result of leakage current that flows in sub-threshold operational areas. Due to its enhanced channel flexibility and

improved gate control without sacrificing efficiency, FinFET semiconductor technology has an important chance to replace CMOS technology in more current SRAM [6]. Additionally, in the sub-threshold region, the leakage current in FinFET is often lower than that in MOSFET. In comparison to CMOS transistors, the FinFETs having lower short channel impact, leakage power, and leakage current and are readily scaleable.The voltage of the supply has to be lowered as technology becomes even more advanced so that dynamic electricity can be maintained. But as a consequence of scaling, leakage current causes an increase in power usage. Therefore, accurate estimation and reduction of leakage power dissipation, particularly for low power applications, depend on the precise identification and modelling of numerous leakage constituents. Several techniques are employed to reduce power consumption while maintaining rapid speed [7]. The significant SVL circuit type not only reduces power consumption but also enhances acceleration. When switching among active mode and silent mode, the efficiency of operation is maximised by creating the maximum or minimum supply voltage and the minimum or maximum ground voltage.

2. LITERATURE SURVEY

The Galeor approach, whose depends on the introduction of one gate leaking high VT nMOS transistor among output and the pull-up network and controlled leakage high VT Pmos among output transistor and full-down network, was recently evaluated by Anitha K et al in February 2016 [8].However, this method is hampered by a low voltage swing and a long propagation delay. In order to address these issues, they presented the Enhanced Galeor Leakage Reduction Technique, whereby combines the Galeor method with a shunt regulator. This has resulted in a forty percent decrease in leakage current. Drowsy Cache technique was developed by Dinesh Chand Guptaet.al [9]. Whenever simply data preservation is needed, this method places memory in low VDD. Whenever genuine data transmission occurs, it provides high VDD.This lessens power leakage and consequently leakage current. They have utilised VDD = 1V for regular operation and 500 mV for keeping information in their suggested work. Dual Vt and dual tox assignment approaches were employed by Amelifardet al. in July 2006 to lower the overall leaking power dissipation of SRAMs without preserving their efficiency [10]. The suggested approach is founded on the finding that the physical separation between the memory cell and the sense amplifier and decoder affects its read and write latency in an SRAM block. The suggested approach does not have any area or latency above you, in contrast to current methods for low-leakage SRAM design. Additionally, it causes a modest modification to the SRAM design flow. Outcomes from simulation using a 65 nm process has incontestable to demonstration that this skillfulness can decrease the total leakage power dissipation of a 64 Kb SRAM by more than 50%. By combining two key concepts, Shin-Pao and Cheng Shi-Yu Huang [11] provide a low-power SRAM implementation utilising quiet-bitline architecture. Initially a one-side driving strategy for the write operation to avoid overcharging the bitlines with full swing. The read operation should also use a precharge-free pulling technique to maintain low voltages on all bitlines at all times. The immediate advantage of changing the two separate write and read procedures is that all the consumption of power related to the bitlines might be drastically reduced. Both the write and reading commands must be changed to do this.

Row-by-row variable voltage method, suggested by K. Kandaet al. in 2002, can minimise active power leakage over an additional order of magnitude [12]. The loss of power of memory cells becomes the main problem in a voltage area of less than 1 V, where the VTH is reduced to less than 0.2 V. Using the drain inspired barrier lowering (DIBL) effect, the supply voltage of unaccessed cells may be continuously dropped, row by row, thereby dramatically reducing cell leakage. Unaccessed word lines are stimulated using a negative voltage in addition to an altered swing write approach to further decrease the leakage between bitline via transfer gates of memory cells. The biggest disadvantages of this approach are that, similar to the changing VDD scheme, there's dynamic power expenses and an additional voltage generator is required to supply the negative voltage, which causes the gate current leakage of access transistors rising.

SVL TECHNIQUE FOR LOW POWER Fin FET BASED SRAM

The primary focus of this research is on FinFET-based SRAM cell design with the SVL approach for reduced leakage power dissipation. This work considers a new 7T FinFET SRAM cell exhibiting very low leakage current and power using SVL approaches. Three methods can be used to apply SVL methods: Lower SVL, upper SVL, and combination SVL are the first three.

Development of an SRAM cell using FinFET Utilising the Cadence design tool, Figure 1 depicts a 7T FinFET-based SRAM cell that is built for the 18 nm technological node.The seven transistor SRAM cell that is being shown makes use of a one-bit line (BL), a word line (WL), and a read line (RL). Yet

Bit-line (BL), word-line (WL), and read-line (RL) are all used when writing data into the cell; read-line (RL) is not used (inactive). Additionally, bit—line (BL), read line (RL), and idle word-line (WL) are all used while reading from a cell. The 7T SRAM cell uses just one bit line, word line, or read line for each specified operation.

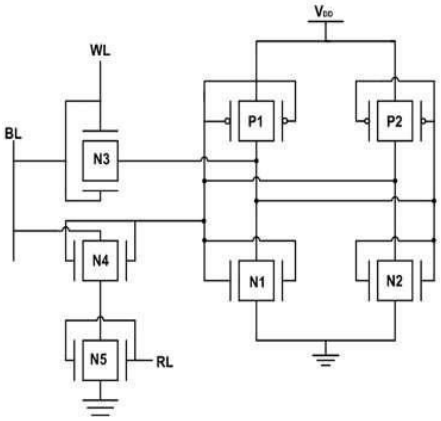


Fig.1:7 TFin FET depending SRAM Cell

SVL TECHNIQUE

Switches in the SVL circuit are in the weak reversing area whenever their threshold voltages (Vth) and gate voltages (Vgs) are below each other. As a result, the substrate's p type voltage rises and the drain source voltages (Vds) of the "OFF-FinFETs" in the reserve load circuits diminish. This raises the threshold voltage, which causes the sub threshold current impedance of the "OFF-Fin FETs" to decline. This reduces power while preserving data. SVL switch is used either above the cell (USVL switch) to decrease supply voltage in standby state or below thecell (LSVL switch) to increase the potential of ground node in stand by state or as a combination of both. Upper Self- Controllable Voltage Level (USVL): The USVL switch, named here astype-1 SVL switch, consists of only one P-channel FET transistor switch (p-SW)and series combination of 2 NMOS switches (n-SW). The FinFET-based 7T SRAM cell incorporating SVL (USVL) circuits is shown in Fig. 2. On solicitation, the ON p-channel FinFET transistor connects to a power supply VDD and a 7T SRAM cell built on a FinFET in the dynamical mode, and the ON n-channel FinFET transistor connects to a power supply VDD and a 7T SRAM cell in the sleep mode. In this method, the supply voltage to the FinFET-based 7T SRAM is reduced to voltage level VD in sleep mode whereas a full supply voltage (VDD=1 V) is linked to the FinFET-based 7T SRAM cell in dynamic mode. First, we assess the effect on current leakage.

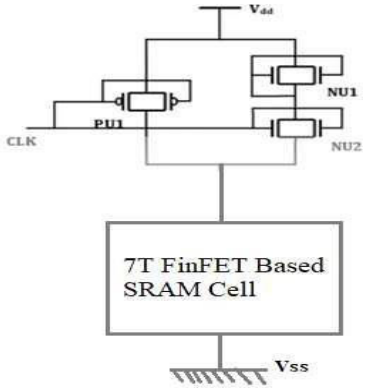


Fig. 2: 7T FinFET based SRAM using USVL Simulated gate voltage of transistor M6 indicates reduced gate leakage current across it. Due to a decline in transistor N1's channel voltage, transistor N2 has a lower gate channel voltage crosswise, which also results in a reduction in gate current leakage. Transistor N4's gate leakage current is unaffected. Utilising the USVL circuit, the p-channel FinFET transistor PU1 does not have substantial leakage current. A better way to lessen leakage current is via USVL. In any event, this approach is inferior to the sub-limit leakage current in terms of difference. The transistors N1, P2, and N4 reduce the sub-edge leakage current, but the cross-sectional pattern of the current leakage is unaffected. The two gate leakage current in access transistors N3, N4 remains unchanged, and this process is gradually effective in decreasing gate leakage current, to list all the effects of the USVL method. Lower Self-Controllable Voltage Level (LSVL): The LSVL circuit is made up of one n-channel FinFET transistor, two p-channel FinFET transistors arranged in a group, and it is placed among a 7T SRAM cell that operates on FinFETs and a ground-level power supply, as demonstrated inFig.3.

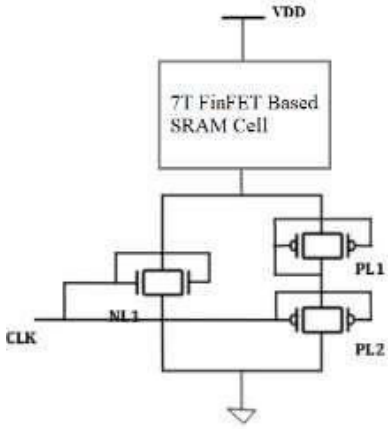


Fig. 3: LSVL-based 7T FinFET-based SRAM The M8 transistor in the LSVL circuit supplies Vss to the 7T SRAM cell, and the additional 7T SRAM cells are also supplied with Vss utilising the PL1 and PL2 transistors. Due to the LSVL circuit (Fig. 3), which connects 0 V to the 7T SRAM cell's control signal (CSB), M10 transistor turns on and NL1 turns off, causing Vss to be linked to the 7T SRAM cell. The CSB switch provides 0 V at ground potential in dynamic operation and a higher simulated ground in idle mode. LSVL reduces leakage from N1, P2, and N4 as a result. All sub-threshold values may be represented as the technique's output:In a USVL+LSVL system, both approaches have been applied to a FinFET-based 7T SRAM cell, resulting in a reduction in supply voltage and an increase in ground node voltage, that improves results in lowering leakage current, leakage voltage, and leakage power. Figures 4 show the circuit diagram of a 7T SRAM cell built on FinFETs that uses mixed techniques (USVL and LSVL).

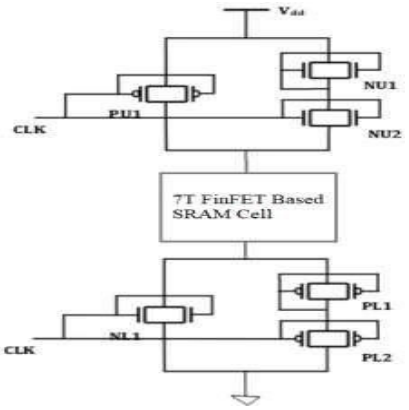


Fig.4: 7 TFinFET based SRAM using combined SVL

Switches get turned on and off according to the input signal given to clock (CLK) which acts as a kind of control signal in active mode. In USVL system when CLK is 1, PU1 gets turned off and NU1, NU2 gets turned on weakly as a result of which VDD is provided directly throughout weakly ON switches and likewise in LSVL system CLK is 0, PL1, PL2 are turned ON weakly and NL1 gets OFF as a result of that VSS is supplied to stand by SRAM.

RESULTS

First of all, analysis of a SRAM cell is done. Gate and sub-threshold leakage currents are evaluated so that comparisons can be made hence forth. Supply voltage is taken 1.1 V.First, data is written in the cell and then the cell is operated in stand by mode. In the following analysis, value stored in Q is _0‘.It is done by providing BL as _0‘ and BLBas _1‘, while providing _1‘ to word line WL(to turn ON the access transistors). After the data is stored, cell is operated in stand by mode, which is done by pre charging both Bl and BLBi.e. both BL and BLB are made _1‘ and word line WL is provided with a‘0‘.Now, average values of gate and sub-threshold leakage currents are evaluated. Value of static power is also recorded. Stand by power of this SRAM cell is obtained as 20.350 nW. Gate leakage and sub-threshold leakage of the cell is obtained as 22.187pA and33.159nA respectively. To reduce stand by power and leakage currents, SVL technique is applied. The examination of the SRAM cell's leakage current utilizing SVL methodologies is shown in the accompanying Table 1, along with comparisons to CMOS and FinFET alone.

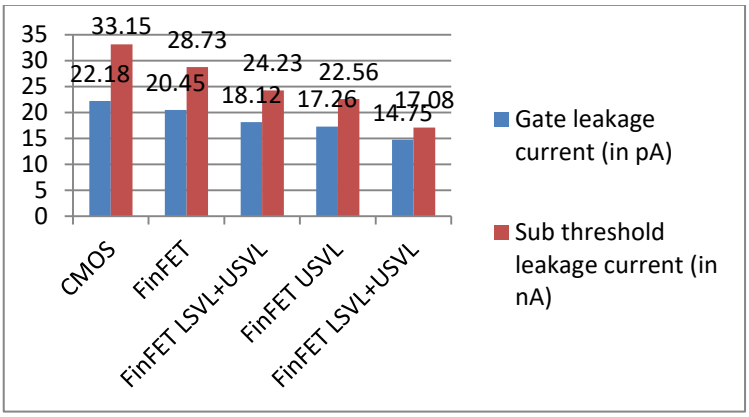


Figure 5: Leakage Current Analysis of SRAM Cell Using SVL Techniques

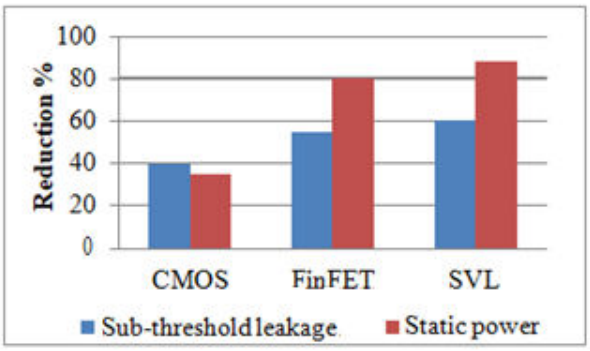
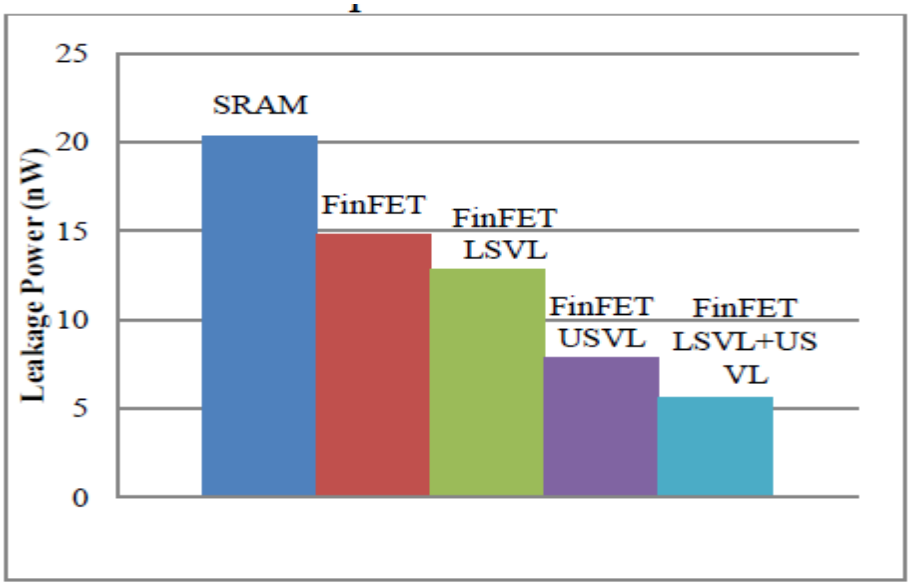


Fig. 6: Reduction (%) of Leakage power and currents using different technique

SVL approach is particularly effective for reducing leakage and static power while retaining high speed performance, according to the findings made. USLV is more effective than LSVL for leakage reduction as NMOS have lower ON resistance. The optimum method for reducing leakage and static power turns out to be combined. NThe overall percentage (%) of decrease in Sub-Threshold-Leakage Current and Static Power is displayed in Figure 5 when CMOS, FinFET, and SVL are applied to SRAM. The largest reduction in Sub-Threshold-Leakage Current and Static Power is obtained in SVL Technique in comparison to CMOS and FinFET.



The Fig.7 Shows the comparative results of leakage power analysis of SRAM using Different Techniques. It can be seen that More leakage power is observed in CMOS technique where as Low leakage power is observed at FinFET based LSVL+USVL technique.

CONCLUSION

An SVL-based method for low leakage power SRAM cells employing FinFET devices is suggested in this paper. In this research, SVL method leakage parameters of 7T SRAM Cell have been computed. This paper employs three different SVL circuit types to lessen leakage in FinFET devices. Leakage current and leakage power were discovered to be lowered by using the SVL method, and to further decrease them, the LSVL, USVL, and combination methods been presented. These significantly decreased the leakage in FinFET-based SRAM cells. The access control transistors remain OFF in IDLE mode in both LSVL and USVL, and the ground potential was correctly preserved even when the voltage was decreased. According to simulation results,

the greatest decrease percentages for leakage current and leakage power in the SVL method used 7T FinFET SRAM cell are 60% and 88%, correspondingly. This comparison demonstrates that employing the SVL technique to create FinFET-based 7T SRAM cells might be preferable over employing traditional CMOS and FinFET-based 7T SRAM cells.

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