# ANALYSIS ON EMPLOYING THE IC 7483 DIGITAL ADDER IC, THE XMM1 MODEL FOR MEASURING THE POWER ON MULTISIM SOFTWARE

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#### ABSTRACT

An adder- subtractor in a digital circuit is one that can perform addition and subtraction of operators inside the same circuit. It is one of the ALU's components (Arithmetic Logic Unit). In order to accomplish both operations on a single circuit while using less power and complexity, we are creating a 64 bit adder-subtractor circuit based on a 4 bit adder-subtractor circuit. Thus, adopting MULTISIM SOFTWARE is a viable option. The ALU of computers frequently uses adders and subtractors to simplify the circuit design. Adder and subtractor are mostly utilized in electronic calculators and digital instruments to conduct arithmetic operations like add and subtract. Digital calculators employ adders for addition and subtraction operations that require some sort of adder-subtractor circuit. XMM1 model will be used in this project for measuring the power on a multisim software. IC 7483 is a digital adder IC that can add two 4 bit numbers. IC 7483 consists of four individual full adder circuits which are internally connected. It has also input and outputs carry circuit.

Key words: Adder-Subtractor Circuit, Multi sim Software.

#### 1. INTRODUCTION

Because of the circuit's increasing speed and complexity as well as the rising need for portable devices like laptops and mobile phones, power consumption in today's VLSI design circuits has increased significantly. The importance of power-efficient circuits can be highlighted. Create adders as the fundamental building blocks of the intricate mathematical circuit. For the construction of addresses in cases of cache and memory access, the CPU, ALU, and floating point units are frequently employed, and digital signal processing is also involved. having quick adding operations and little power usage. For evaluate the power readings measurement, we required multimeter for power readings. Generally A multimeter measuring instrument that can measure a multiple electrical properties.

#### EXISTING METHOD

We have 4bit full adder and full Subtractor these two methods only can adds and Subtracts 4bits of data and we can also perform combination of both addition and subtraction by using 7483 IC Fig:4 bit full adder







Schematic View of 64 bit full adder-subtractor



#### PROPOSED METHOD

Here we proposed a 64 bit full adder subtractor circuit in order to reduce the power consumption and to add or subtract 64 number of bits An 64 bit adder- Subtractor is a digital circuit that produces the arithmetic sum and subtraction of 64 bits of two operands. It can be constructed with 16 of 4 bit IC7483 for performing both adder

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. and subtractor operation in an one circuit, with the output carry from each IC adder connected to the input carry of next IC adder in chain. The augends bits of 'A' and the addend bits of 'B' are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bits. The carries are connected in chain through the full adder. The input carry to the adder is C0 and it can be ripples to the above full adders to the output carry C4. So by reducing the number of transistor we can design the low power area.

## DESIGN OF THE PROPOSED METHOD

For an 64 bit adder subtractor circuit we are using 16 of 4 bit 7483IC. By this we can send the first carry output to next 4 bit adder subtractor circuit. Again this second output is send it to the next third 4bit adder subtractor circuit. so this process we will continue up to the last 4 bit adder subtractor circuit. Based on performing the addition and subtraction operation, we can hold the control bit by either 0 or 1.

## A0,A1,A2,A3......A63 and B0,B1,B2,B3.....B63

Let us assume the control bit k. If the control bit k=0, 0 means addition operation should done. So the add operation will be done between the two operands of 64 bits. This shows on Hex display. Now if the control bit k=1,1 means it will perform subtraction operation. So Between the two operands of 64 bits, subtraction will be done and shows the binary output in hexadecimal value in hex display



## ADVANTAGES

The below following points are the advantages that comes from this 64 bit adder-subtractor circuit:

- VLSI system and design trend is moving away from speed constraint to power due to the rapid technology evolution growth in the portable consumer electronics market.
- Aadder- subtractor using XOR gates which are in turn designed with less number of transistors is implemented. So it will be useful for a long time.
- Multi sim software used by this circuit which is a free of cost implementation.
- Easily done the both operation in one circuit to reduce the time.
- It is easy to perform the arithmetic operations in an micro processor.
- For an more number of bits we can use it also low power are applications so there is no need to use high power..
- The main advantage is to add or subtract is easy for amore no of bits.
- It offers a low power.

## APPLICATIONS

- This can be applicable to low power are a applications.
- Adders are used in digital calculators for arithmetic addition and devices that uses some kind of incrementor arithmetic process.
- They are also used in microcontrollers for arithmetic additions, PC(program counter) and timers.

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- It is also used in processors to calculate address, tables and similar operations.
- It is also used in networking and DSP (Digital signal processor) oriented System. It is also used in Central processing units.

### **RESULT AND DISCUSSION**

As a result, we successfully get low power from our designing64 bit full subtractor adder circuit. This be implemented on a multi sim software. so Finally we get the results Has a lowpowerwhichis888.178nA

## COMPARISONTABLE

Adder and Subtractor Type	Voltage(v)	Current(i)	Power(v*i)
4 bit full adder			
	12v	163.52mA	1.962uW
4 bit full			
Subtractor	12v	179.32mA	2.152uW
64 bit full adder			
	12v	895.46mA	10.74uW
64 bit full			
Subtractor	12v	953.67mA	11.44uW
64 bit			
Full adder-	12v	858.89mA	10.30uW
subtractor			



#### CONCLUSION

Conclusion For more No of processing operations like multiplications, Filtering etc., These addition forms the foundation. Pass transistors are very powerful for designing such efficient XOR gate which is used in adder circuits. The lay out of all the designs are simulated here using MULTI SIM tool. The draw back comes from the 4 bit adder subtractor circuit, we cannot use itto low power applications and also if we want to applied to more number of bits it doesn't support so, for weare designing a 64 bit adder -subtractor circuit which is capable to apply amore number of bits and also this can be applicable to low power are a applications. And we success fully desired our project output.

#### Future scope

In future, This work can be carried out to high speed applications. As an attempt to develop In the future, this will strive to explore and construct more excellent adder-subtractor circuit in order to provide basic module for the larger–scale arithmetic operation. However, there are limitations in our work and several future research directions are possible.

#### REFERENCES

- 1. Digital Electronics, Principles, Devices and Applications, by Anil.K.Mainipp245-246
- M.B.Damle, Dr.S.SLimaye, M.G.Sonwani, "Comparative Analysis of Different Types of Full Adder Circuits" IOSR Journal of Computer Engineering (10SR-JCE)-ISSN:2278-8727Volume11,issue3, 2013, PP01-09.
- 3. Chetana Nagendra, Mary JaneIrwin, RobertMichael Owens "Area-Time-Power Tradeoffs in Parallel Adders" IEEE Transactions On Circuits And Systems ANALOG AND DIGITAL SIGNAL PROCESSING,vol43,NO.10,OCTOBER1996.