MODELLING OF A HIGH PERFORMANCE AND HARDWARE EFFICIENT MAGNITUDE COMPARATOR: AN ANALYTICAL STUDY

[1]C.Vidya, [2]Sk.Jakeer Hussain, [3]S.Jagadeesh, [4]Chevuru. Venu

[1,2,3]Dept of Electronics and Communication Engineering, Sree Venkateswara College Of Engineering, Nellore (Dt), Andhra Pradesh, India.

[4]Dept of Computer Science and Engineering, Sree Venkateswara College Of Engineering, Nellore (Dt), Andhra Pradesh, India.

ABSTRACT

This paper presents a hardware-efficient, high-performance magnitude comparator. Here, there are two modules that have been split once more into various numbers of sets. CEM (comparison evaluation module) and FM are these modules (final module). There are 5 sets in all, with sets 1-4 being CEM and set 5 being FM. A parallel prefix tree-like structure may be found in the CEM. Each set makes use of many gates, including nand, novel, exor, etc. The analytical derivation of area is in terms of the transistor count due to the huge topology in the structure. We used various tools to develop the suggested comparator utilising 180nm technology. Low input-output delays, low power consumption, and full swing output voltage are this method's key benefits.

INTRODUCTION

A magnitude comparator/digital comparator is used for comparison of two operands the comparison results may be one of these: A>B,A=B,A<B when A and Bare compared.

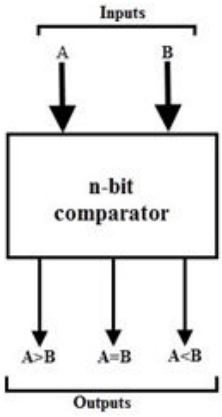


Fig.1. Basic comparator

The comparator can be used for scientific computations such digital image processing, pattern recognition, matching, and for self-test circuits that are built-in. The central processing unit also makes advantage of it.We need an IC chip that is as compact as possible so that it may be inserted in any other device because it has a wide range of applications and requires a high-speed and area-efficient comparator. Therefore, the comparison tool's design is crucial. The comparator should not only be compact but also operate at a quick rate. The foundation for it has been set by CMOS technology. We can create fast and space-efficient comparators by employing it.

EXISTING METHOD

In the existing method, we have the same two modules that is CM (comparison evolution module) and FM (final evolution model). The set one of CEM is a 8T transistor model. As a CMOS logic is being used for this method the power consumption and speed are better than the previous method. In the existing method, we are able to

produce output at good speed when compared to the previous methods, but the output full swing voltage is not obtained. This is one of the major drawbacks of the existing method. We can further reduce the power consumption, delay and can produce output full swing voltage by using our proposed method.

PROPOSED METHOD

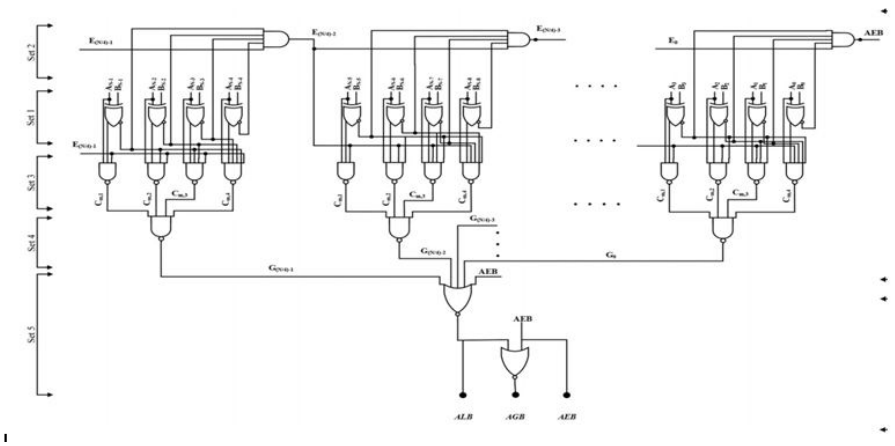
The suggested method modifies the current method by altering the evolution module for set-1 of comparisons. As we already discussed, set-1 of comparison evaluation model in existing method has 8 Ttransistor logic, We are going to replace it with a 7 T transistor logic.

To do so, we'll use a unique EXOR-EXNOR gate to lower the number of transistors in the set-1 comparison evolution module. So that it is possible to decrease the number of transistors employed in the proposed approach CEM and FM structure of the proposed method fig. The higher-level and lower-level architectures are represented by the modules.

The CEM has a parallel prefix tree structure that is utilized for comparing two N-bit operators A and B bitwise. In the suggested technique. Although the output full swing voltage cannot be achieved, we can further lower the transistor count by using 6T transistor logic. In order to get the best speed and area efficiency, we therefore favour 7T transistors.

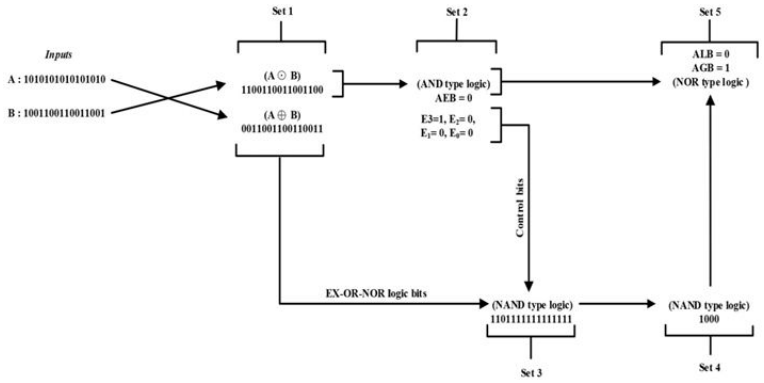
The following fig.3 shows the proposed NOVEL EXOR-ENOR gate

Here we are obtaining an output of EXOR and ENOR The full swing voltage is obtained due to the presence of M5 transistor. The outputs of set-1 are further given to set-2 and set-3.The outputs of set-3 are sent to set-4 in the form of nibbles. Further the values of set-4 are then finally sent to the set-5, which is the final comparison module that produces the final output (A=B,A>B,A<B).



IMPLEMENTATION OF THE PROPOSED METHOD

The better understanding of the implementation of the proposed method is shown the the fig.4.Here 2 operands are compared in different sets at a time to produce the result by using the parallel prefix tree structure. The operands A and B are given to the set1 which produce ex-nor and exor outputs which are passed to set2 andset3.The output of set2 are passed to next parallel part and output of set3 is passed as input for set4 in the form of nibbles. This output is finally passed to set5 which is used for final comparison of the operands. The implementation of proposed method fig-4



APPLICATIONS

1. It can be used for scientific competitions
2. It also can be used in digital image processing or matching.
3. It is used in built in self test circuits.
4. It is also used in Central processing units.

RESULTS

We can create a highly effective comparison using the approach we've suggested. This is applicable to nbits.The schematic diagram for our suggested approach using a 64-bit comparator has been constructed and can be seen in the figure below in figure 5.

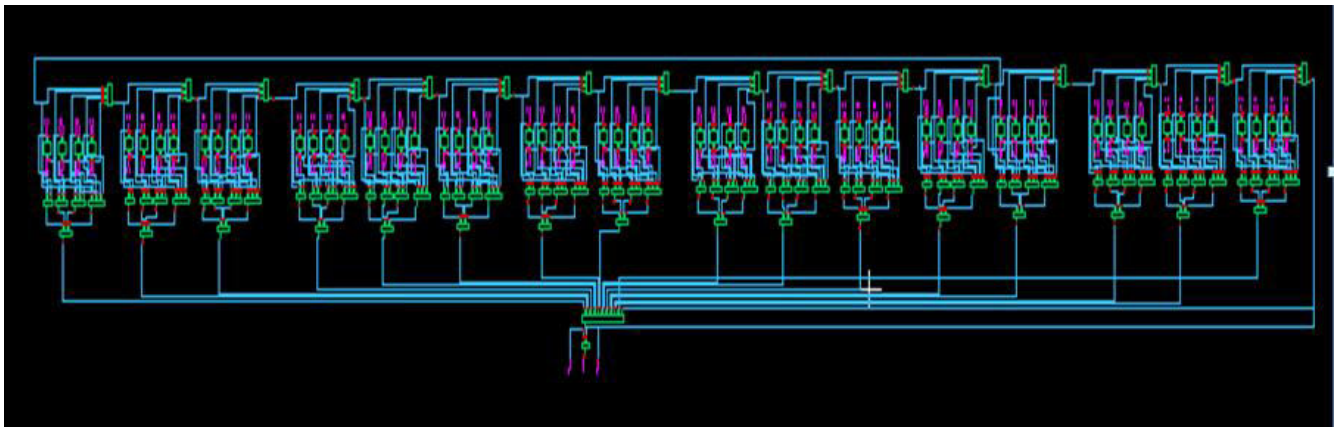
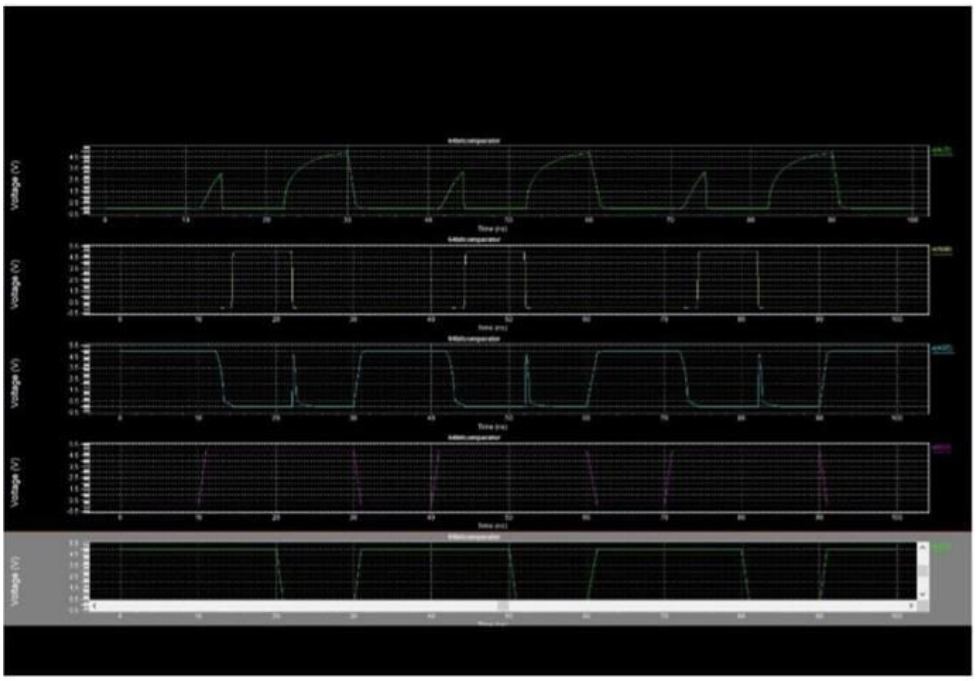


fig.5

The block diagram of fig 2 has been used as the base to design tanner tools' 64-bit schematic diagram Novel gates, gates, nand gates, and xor gates are all implemented in the schematic diagram in various sets. With the exception of set 1, which uses operands as inputs, the outputs of previous sets serve as the inputs for subsequent sets.

OUTPUT WAVEFORM

The output waveform of the executed schematic diagram following execution of the input code in Int-Spice is shown in Fig. 6 below. We can see from the waveforms that the full swing output voltage. In the output display we can also observe the delay and the power consumption i.e. in the software. The output wave forms. Fig.6



COMPARISON TABLE

Factors	Existing method	Proposed method
Area (in transistor count)	1588	1524
Power consumption	9.4mW	5mW
Delay	10ns	4.34ns

CONCLUSION

Some more proposed method you overcame the drawbacks of the existing method by replacing the 8T transistor logic to 7Tnovel EXOR-EXNOR transistor logic. As the transistor count is reduced, The critical path of the output is also reduced, Therefore the speed of execution has increased. By using theM5 transistor in the novel EXOR-ENOR gate, we are able to produce the full swing output voltage. By this we can say thatwehaveovercamethedrawbacksoftheexistingmethodusingourproposedmethod

Future scope

- The proposed comparator has wide range of applications.
- It involve scientific computations (digital image processing, pattern recognition/ matching, arithmetic sorting).
- It is also used for data compression and digital neural network and test circuit applications (built-in self-test circuits, signature analyzers and measurement).
- A digital logic can be used instead of CMOS to reduce power consumption.

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